

**REMARKS**

Claims 1-13 are pending. Claims 10-11 have been canceled.

Claims 10-11 stand rejected under 35 USC §102(b) as being allegedly anticipated by Kishino (US 5,153,483).

Claims 1 and 3 stand rejected under 35 USC §102(b) as being allegedly anticipated by Cathey (US 5,844,370).

Claims 1, 3, and 8 stand rejected under 35 USC §103(a) as being allegedly unpatentable over applicant's admitted prior art in view of Cathey (US 5,844,370).

Claims 2-7, 9, 12 and 13 are objected to but would be allowable if rewritten in independent form.

**Changes in the Drawings:**

The drawings have been amended in response to the Examiner's request for the purpose of overcoming the Examiner's objection. Specifically, FIGS.1-5 stand objected to on the grounds that the legend "Prior Art" is missing. MPEP §608.02(g). FIGS. 1-5 have been amended to be designated with the legend "Prior Art." Applicant therefore requests that the objection to the Drawings be withdrawn.

No new matter has been added. Approval of the corrections is respectfully requested.

**Changes in the Specification:**

The specification has been amended for the purpose of improving the readability of the application and are of a clerical, typographical or grammatical nature. No new matter has been added.

Specifically, the specification has been amended in response to the Office Action's guidelines for the preferred layout for the specification. No new matter has been added.

**Changes in the Abstract:**

The Abstract has been replaced in response to the Office Action's suggestion for the proper language and format.

**Changes in the Claims:**

Claims 10 and 11 have been canceled.

Claims 1-9, 12-13 have been amended in this application to further particularly point out and distinctly claim subject matter regarded as the invention. No new matter has been added.

**Rejection under 35 USC §102(b) – claims 10-11**

Claims 10-11 stand rejected under 35 USC §102(b) as being allegedly anticipated by Kishino (US 5,153,483). Claims 10 and 11 have been canceled. This rejection is therefore moot.

**Rejection under 35 USC §102(b) – claims 1 and 3**

Claims 1 and 3 stand rejected under 35 USC §102(b) as being allegedly anticipated by Cathey. This rejection is respectfully traversed.

A claim must be anticipated for a proper rejection under §102(a), (b), and (e). This requirement is satisfied “only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference”; see MPEP §2131 and *Verdegaal Bros. V. Union Oil*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1984). A rejection under §102(b) may be overcome by showing that the claims are patentably distinguishable from the prior art; see MPEP §706.02(b).

Cathey describes a field emission display that includes electrostatic discharge protection circuits coupled to an emitter substrate and an extraction grid. See Abstract of Cathey.

In contrast, the presently claimed invention claims “the commutation component (18,20) is integrated through design in the first substrate (2) and in the second substrate (12) of the screen (1).” See claim 1. Cathey does not teach or suggest building the commutation component (18, 20) into the first substrate (2) and in the second substrate (12) of the screen (1). Instead, the high voltage ESD diode (120) is not a commutation component since it is used for protecting the transparent anode (54) against electrostatic discharge (See column 5, lines 40-44 of Cathey). In the presently claimed invention, the transistor (18, 20) is a commutation component used for monitoring the screen (See specification at page 11, line 1-10).

The presently claimed invention is, accordingly, distinguishable over the cited reference. In the view of the foregoing, it is respectfully asserted that claims 1-10 are now in condition for allowance.

**Rejection under 35 USC §103(a) – claims 1, 3, and 8**

Claims 1, 3, and 8 stand rejected under 35 USC §103(a) as being allegedly unpatentable over applicant's admitted prior art in view of Cathey (US 5,844,370). This rejection is respectfully traversed.

Under MPEP §706.02(j), in order to establish a prima facie case of obviousness required for a §103 rejection, three basic criteria must be met: (1) there must be some suggestion or motivation either in the references or knowledge generally available to modify the reference or combine reference teachings (MPEP §2143.01), (2) a reasonable expectation of success (MPEP §2143.02), and (3) the prior art must teach or suggest all the claim limitations (MPEP §2143.03). See In re Royka, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974).

Cathey describes a field emission display that includes electrostatic discharge protection circuits coupled to an emitter substrate and an extraction grid. See Abstract of Cathey.

The proposed combination of Applicant's admitted prior art with Cathey does not teach or suggest "the commutation component (18,20) is integrated through design in the first substrate (2) and in the second substrate (12) of the screen (1)." See claim 1. Instead, the high voltage ESD diode (120) is not a commutation component since it is used for protecting the transparent anode (54) against electrostatic discharge (See column

5, lines 40-44 of Cathey). In the presently claimed invention, the transistor (18, 20) is a commutation component used for monitoring the screen (See specification at page 11, line 1-10).

Applicant therefore submits that the rejection based Applicant's admitted prior art and the Cathey reference is improper and should be withdrawn. Thus, Applicant submits that claims 1, 3, and 8 recite novel subject matter which distinguishes over any possible combination of Applicant's admitted prior art and the Cathey reference.

### **Conclusion**

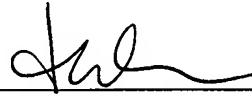
For all of the above reasons, applicants submit that the amended claims are now in proper form, and that the amended claims all define patentable subject matter over the prior art. Therefore, Applicants submit that this application is now in condition for allowance.

**Request for allowance**

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited. If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Please charge any required fee or credit any overpayment not otherwise paid or credited to our deposit account #50-1698.

Respectfully submitted,  
THELEN REID & PRIEST LLP



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Attachments



ANNOTATED MARKED-UP DRAWINGS

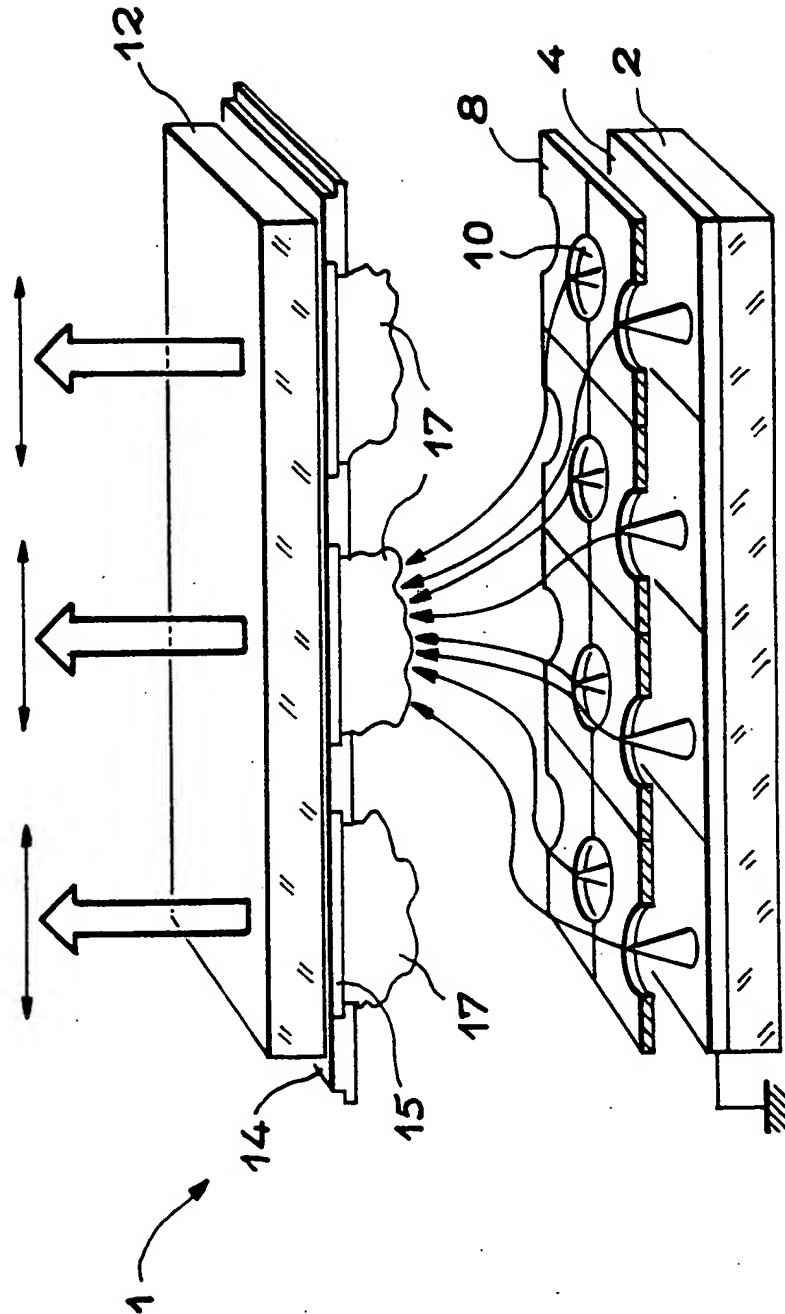


FIG. 1  
PRIOR ART

The schematic diagram illustrates a thin-film transistor (TFT) array circuit. A gate voltage pulse \$V\_1\$ is applied to a gate electrode (26) through a resistor (24). The TFT (18) has its source connected to ground and its drain connected to a load resistor (40) and a storage capacitor (50). The gate voltage \$V\_{g1}\$ is controlled by the input pulse \$V\_1\$. The drain voltage \$V\_{d1}\$ is determined by the HT (high threshold) level. The output signal is taken from the drain terminal (20) through a resistor (22). The gate voltage \$V\_{g2}\$ is controlled by the input pulse \$V\_2\$. The drain voltage \$V\_{d2}\$ is determined by the HT (high threshold) level. The output signal is taken from the drain terminal (20) through a resistor (22).

FIG. 2  
PRIOR ART





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ANNOTATED MARKED UP DRAWINGS

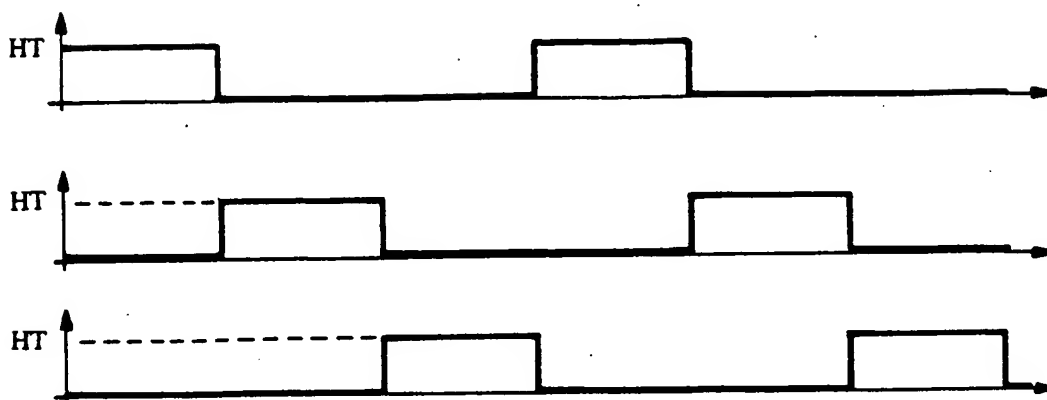


FIG. 3

PRIOR ART



FIG. 4

PRIOR ART

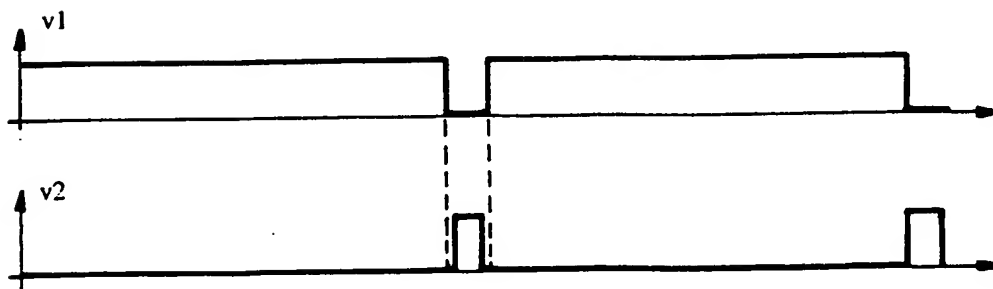


FIG. 5

PRIOR ART

ANNOTATED MARKED UP DRAWINGS

**FIG. 6**

FIG. 6

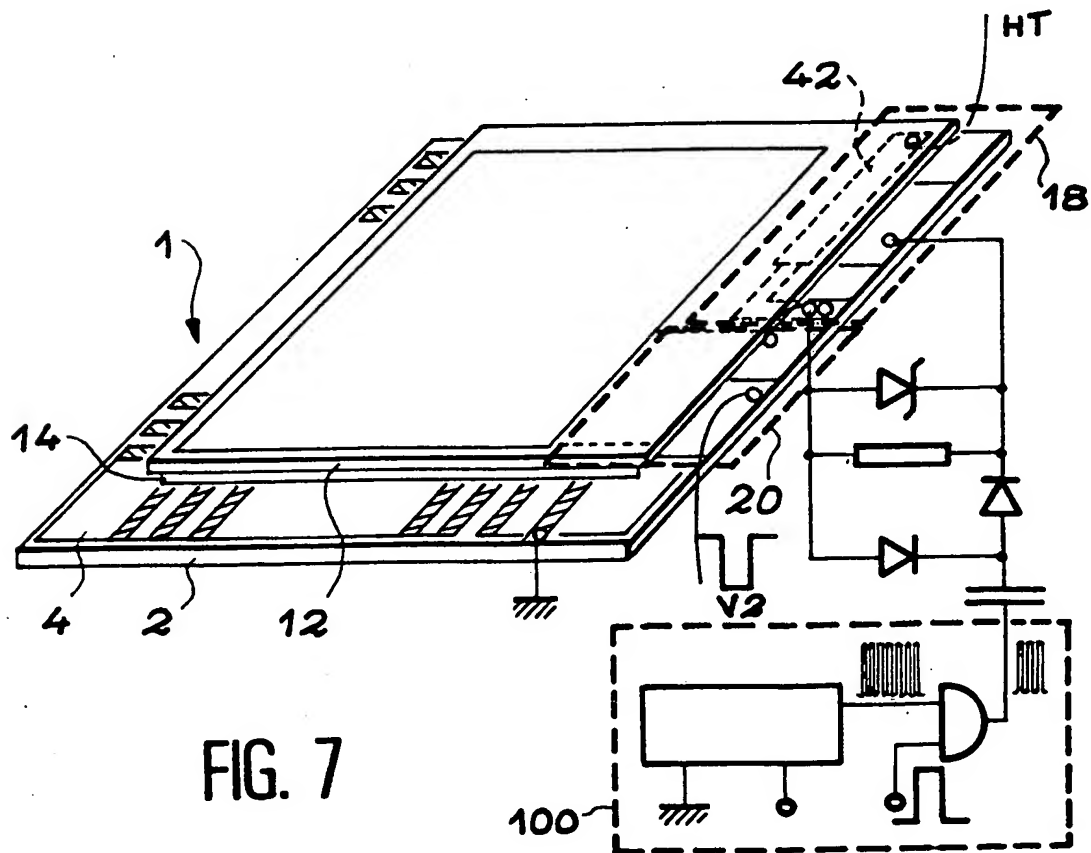


FIG. 7



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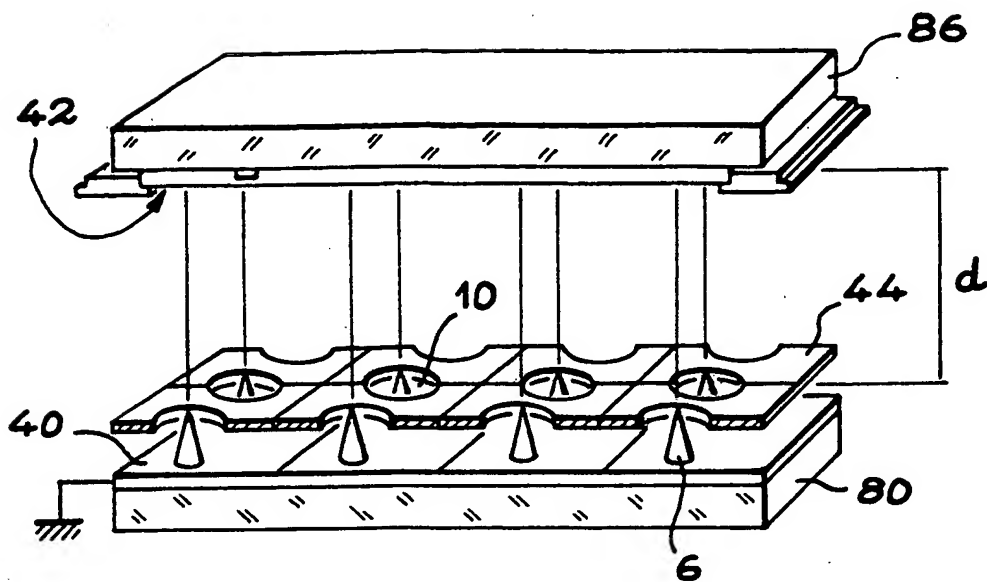


FIG. 8

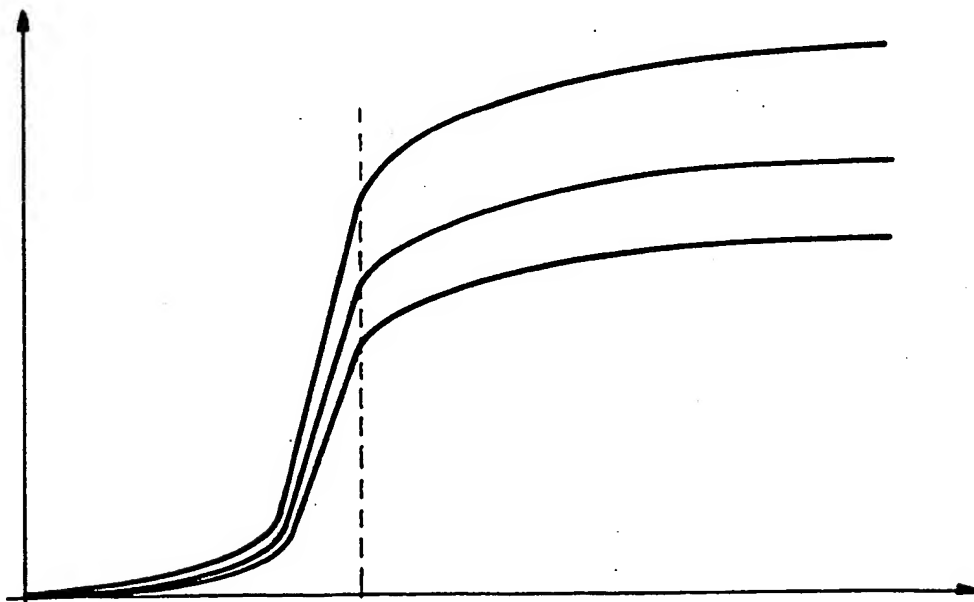


FIG. 9